

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**IN RE APPLICATION OF:
YIN TAT MA**

SERIAL NO. : 10/501,651

FILED: JAN. 10, 2005

**FOR: ON-CHIP ESD PROTECTION
CIRCUIT FOR COMPOUND
SEMICONDUCTOR
HETEROJUNCTION BIPOLAR
TRANSISTOR RF CIRCUITS**

Examiner: D.H. Patel

Group Art Unit: 2836

Confirmation No.: 5137

COMMUNICATION REGARDING EXTENSION OF TIME

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In further reply to the final Office Action mailed February 2, 2007, Applicant believes that the previously filed Requests for Extension of Time and the accompanying fees are unnecessary as Applicant's Reply (received at the PTO on April 12, 2007) to the final Office Action dated February 2, 2007 is well within the shortened statutory period. Applicant's Reply has placed the present application in condition of allowance as confirmed by telephonic communications with Examiner Patel. Thus, the present application would be pending even without the Extension of Time. Accordingly, a Request for Refund has been filed separately.

However, if Applicant's belief is incorrect, the Office is authorized to charge all fees, fees under 37 CFR 1.17, or all required extension of time fees, or any deficit to Applicant's deposit account #01-1960. Applicant also notes that such an authorization has been previously filed on June 28, 2007, and on May 8, 2007 accompanying the Requests for Extension of Time.

If a telephone conversation would be helpful to the prosecution of this case, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please direct all correspondence to **Myers Dawes Andras & Sherman LLP**, 19900 Mac Arthur Blvd., 11th Floor, Irvine, California 92612.

Respectfully submitted,



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